IN THE CLAIMS

1. (Currently amended) A semiconductor device comprising:

a semiconductor substrate;

dummy patterns for a chemical mechanical polishing (CMP) method formed in a uniform pattern over the semiconductor substrate; and

marking patterns that are formed over the semiconductor substrate to correspond to predetermined groups of the dummy patterns,

wherein at least one dummy pattern is formed between two marking patterns,

wherein a number of the dummy patterns is substantially greater than a number of the marking patterns, wherein the marking patterns are smaller than the dummy patterns.

2. (Original) The semiconductor device of claim 1, wherein the marking patterns have a different shape from the dummy patterns.

3. (Original) The semiconductor device of claim 1, wherein the marking patterns have a different size from the dummy patterns.

4. (Canceled)

23. (Previously presented) A semiconductor device comprising:

a semiconductor substrate;

dummy patterns for a chemical mechanical polishing (CMP) method formed in a uniform pattern over the semiconductor substrate; and

marking patterns that are formed over the semiconductor substrate to correspond

to predetermined groups of the dummy patterns,

wherein the marking patterns surround at least a group of dummy patterns, wherein a size of the marking patterns is smaller than a size of the dummy patterns.

24. (Currently amended) A semiconductor device comprising:

a semiconductor substrate;

dummy patterns for a chemical mechanical polishing (CMP) method formed in a uniform pattern over the semiconductor substrate; and

marking patterns that group predetermined plural numbers of the dummy patterns and are formed over the semiconductor substrate;

wherein the marking patterns and the predetermined plural numbers of the dummy patterns grouped by the marking patterns form a unit, which is repeated, wherein the marking patterns are smaller than the dummy patterns.